REMARKS/ARGUMENTS

Claims 1, 5-7, 9, 10, 16, 17, 19, and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Harris; claims 2-4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Harris, and further in view of Ashby; claims 8 and 18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Harris, and further in view of Backus.

Claim 1 comprises the limitations of forming a surface conductive lead in an opening formed within a protective overcoat and over a barrier layer, a portion of the barrier layer extending beyond the surface conductive lead; and subjecting the portion of the barrier layer to a dry etch to remove the portion and form a skirt, the dry etch selective to the barrier layer. In forming the rejection of claim 1 the examiner relies on the Harris reference stating that the Harris reference teaches a method for manufacturing an interconnect for an integrated circuit comprising forming a surface conductive lead (fig. 4, 28a) in an opening of formed within a protective overcoat (24) and over a barrier layer (28b), a portion of the barrier layer extending beyond the surface conductive lead to form a skirt. The examiner is incorrect in this characterization of the Harris reference. The Harris reference firstly does not describe the layer (28b) as a barrier layer. The Harris reference simply describes 28b as a layer of metal. Claim 1 requires the presence of a barrier layer which is a term of art for a layer with a specific function in the claimed structure.

In the action dated 4/11/2007, in responding to the applicant's arguments, the examiner stated that the claims are anticipated by any layer under a conductive lead that prevents direct contact and diffusion of materials with an underlying bond pad, thus acting as a barrier layer. This condition is not satisfied by layer 20b of the Harris reference that the examiner describes as a barrier layer. Referring to the Harris reference, the only description that the applicant can find regarding layer 28b is in col. 3, lines 3-6, where it simply describes 28b as a layer of metal. This description does not satisfy even the examiners stated position of preventing diffusion of metals. It is not

inherent that the layer 20b is inherently a barrier layer. For inherency to be present there must be only one way for the layer 20b to function. This is not the case in the Harris reference. It is possible that the layer 20b will allow inter-diffusion of the various metal species to properly function. The limitation of a barrier layer in claim 1 is neither explicitly disclosed nor is it inherent in the Harris reference.

In describing the motivation to combine the reference the examiner described "reducing the stress on the protective overcoat layer that occurs during packaging of the integrated circuit (Harris, col. 3, lines 21-28), thus reducing the risk of cracking of the overcoat layer and improving device performance". This statement is again a mischaracterization of the teaching in the Harris reference. The Harris reference clearly teaches that reducing the width of the skirt from that shown in Fig 2 (16b) to that shown in Fig. 4 (28b) is responsible for the reduction in cracking. The Harris reference therefore teaches "reducing the width (or base) of the structure rather that the widening of the base to which the examiner refers. The Harris reference teaches away from widening the structure of the instant invention. Furthermore the sections of the Harris reference that the examiner uses to support the rejection are silent on this point. Col. 3, lines 21-28 of the Harris reference describes sizing and placement tolerances sufficient to avoid expanding during the bonding process. Col. 2, lines 41-57 of the Harris reference simply describes the cracking of the structure caused by the position of the skirt of the bump. The Harris reference cannot therefore be properly combined with the Wang reference to reject claim 1 of the instant invention. Pending claims 2-10 depend on claim 1 and therefore contain all the limitations of claim 1. Claims 2-10 are therefore also allowable over the cited prior art.

In the action dated 4/11/2007, in responding to the applicant's arguments, the examiner simply ignores the simple and plain teaching of the Harris reference. The examiner is invited to carefully examine Fig 2(16b) and Fig 4 (28b) where it is clearly shown that it is the reducing of the width to avoid the overlap that results in the claimed advantages of the Harris reference. The Harris reference does not teach that expanding underlying layers to a width greater than upper layers reduces stress. The examiner is

invited to carefully examine Fig 2(16b) where the examiner's stated condition is satisfied and yet there are cracks formed due to stress. This condition negates the examiner's arguments.

Independent claim 16 comprises the limitations of forming a surface conductive lead in the opening and over a barrier layer, a portion of the barrier layer extending beyond the surface conductive lead; and subjecting the portion of the barrier layer to a dry etch to remove the portion thereby forming a skirt, the dry etch selective to the barrier layer. For the reasons stated above claim 16 is also allowable over the cited prior art. Furthermore, claims 17-20 depend on claim 16 and therefore contain all the limitations of claim 16. Claims 17-20 are therefore also allowable over the cited art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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